CLAIMS

What is claimed is:

1. A method of baking a semiconductor wafer substrate comprising the acts of:

(a) baking a substrate coated with a resist at a first temperature for a first predetermined period of time; and

(b) after act (a), baking the substrate coated with the resist at a second higher temperature for a second predetermined period of time.

2. The method, as set forth in claim 1, wherein no resist craters are formed.

3. The method, as set forth in claim 1, wherein during the first predetermined period of time:

the resist hardens; and

the air trapped under the resist does not possess sufficient energy to expand through the resist.

4. The method, as set forth in claim 1, wherein during the first predetermined period of time:

the resist remains fluid;

air trapped under the resist expands through the resist to the surface; and

the resist flows back to its original conformal shape.

5. The method, as set forth in claim 1, wherein the semiconductor wafer is subjected to a temperature in the range of 30-90 °C during the first predetermined period of time.

6. The method, as set forth in claim 1, wherein the first predetermined period of time is less than 90 seconds.

7. The method, as set forth in claim 1, wherein the first predetermined period of time is more than 90 seconds

8. The method, as set forth in claim 1, wherein the higher temperature is in the range of 90-150 °C.

9. The method, as set forth in claim 1, wherein the higher temperature is in the range of 100-130 °C.

10. The method, as set forth in claim 1, wherein the second predetermined period of time is less than 90 seconds.

11. The method, as set forth in claim 1, wherein the second predetermined period of time is more than 90 seconds

12. A semiconductor wafer comprising a resist layer without craters at the completion of a two-part soft bake of the semiconductor wafer.

13. A two-bake system comprising:

a first thermal unit configured to bake a semiconductor wafer coated with resist at a low-bake temperature; and

a second thermal unit configured to bake the semiconductor wafer at a high-bake temperature.

14. The system, as set forth in claim 13, wherein the low-bake temperature is in the range of 30-90 °C.

15. The system, as set forth in claim 13, wherein the high-bake temperature is in the range of 90-150 °C.

16. The system, as set forth in claim 13, wherein the first thermal unit is a hot plate.

17. The system, as set forth in claim 13, wherein the second thermal unit is a hot plate.

18. The system, as set forth in claim 13, wherein the first thermal unit is used to bake the semiconductor wafer at the low-bake temperature for 30-90 seconds.

19. The system, as set forth in claim 13, wherein the second thermal unit is used to bake the semiconductor wafer at the high-bake temperature for 60-90 seconds.

20. A two-bake system comprising a thermal unit configured to bake a semiconductor wafer coated with resist at a low-bake temperature for a low-bake time and at a high-bake temperature for a high-bake time.

21. The system, as set forth in claim 20, wherein the thermal unit is a hot plate.

22. The system, as set forth in claim 21, wherein the hot plate comprises disks for seating the semiconductor wafer.

23. The system, as set forth in claim 21, wherein the hot plate comprises pins for receiving the semiconductor wafer.

24. The system, as set forth in claim 21, wherein the hot plate comprises pins that are extended during the low-bake time.

25. The system, as set forth in claim 20, wherein the low-bake temperature is in the range of 30-75 °C.

26. The system, as set forth in claim 20, wherein the high-bake temperature is in the range of 90-150 °C.

27. The system, as set forth in claim 20, wherein low-bake time is in the range of 30-90 seconds.

28. The system, as set forth in claim 20, wherein high-bake time is in the range of 60-90 seconds.